ECE 544 – Ledit Lecture

Download Instructions

- Access the free student software offered to all UofL Speed School Students
  - https://cardmaillouisville.sharepoint.com/sites/SpeedStudentBundle/SitePages/Student-Software-Listing.aspx

- Download and install Tanner Tools
- Once finished, find the Tanner Tools installation in the Start Menu
  - Open the file inside called “Licensing Software”
  - Select option to obtain license from a server
  - Place this address in the open field: ws225ls.spd.louisville.edu

- Software will only function on your computer when you are on Campus (or UofL VPN)

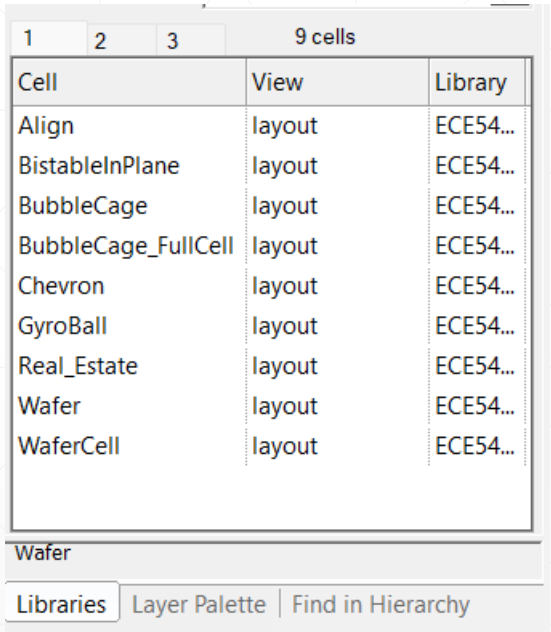
Resources

- New user guide to learn the basics of Ledit
  - https://louisville.edu/micronano/ECE%20544/LeditNewUserGuide.pdf

- ECE544_ClassDemo.tdb
  - File includes a couple of designs used in the first half of the class and can be used for reference when making your own designs

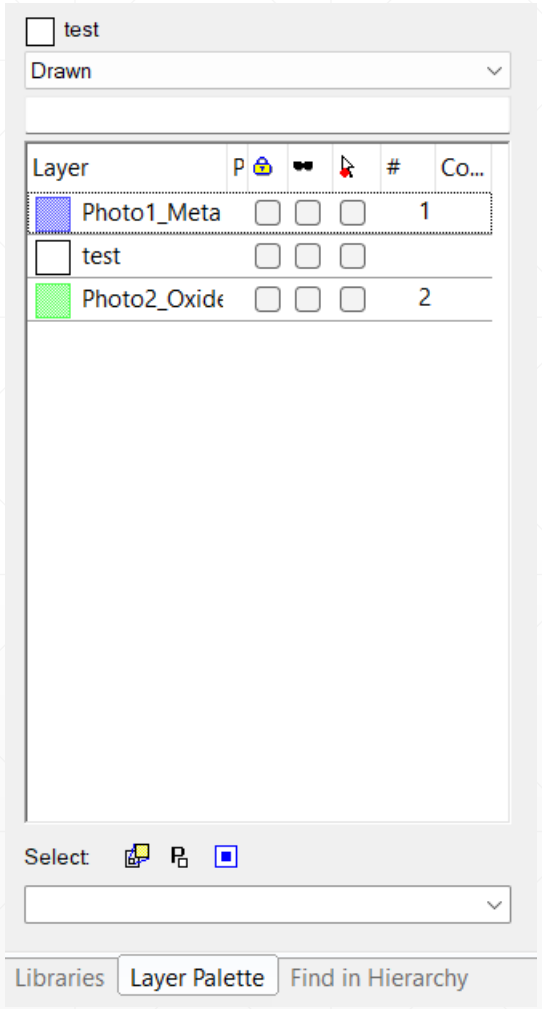
Design Libraries

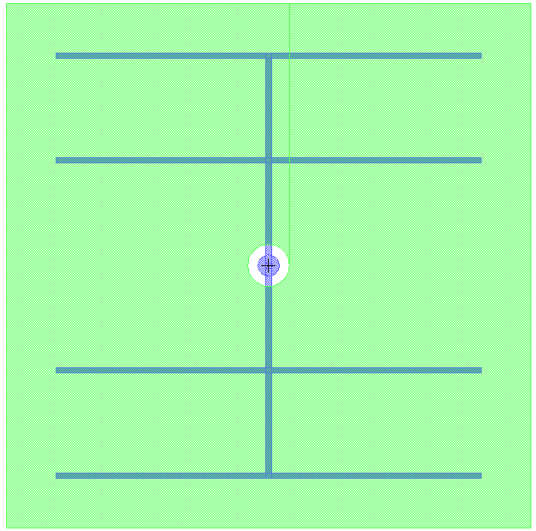
- Show the different cells within the design
- Final design to be printed will be on the “Wafer” cell
  - Changes in the other cells will carry over to the “Wafer” cell automatically if they have been instanced there
- The “Wafer Cell” shows a blank square you can use when laying out your design to ensure it fits on a single die
- Follow the example seen in “BubbleCage”
  - A single instance of the design is written in “BubbleCage”
  - That instance is repeated in “BubbleCage_FullCell” to cover the entire die
- Cells that have been instanced in another cell can be flattened and edited, but this will prevent edits in that other cell from being carried over in the future



Layer Palette

- These are the different layers that can be used in the design
  - The blue “Photo1_Metal” layer shows the areas that will have metal coatings after liftoff
  - The green “Photo2_Oxide” layer shows the areas that will be undercut during the XeF2 etch
  - The empty “test” layer will not be printed at all and is just used to help you visualize and layout your design
- Make sure to consider how the two process layers interact with each other
  - Only layers with both blue and green will release





Final Design

- Create up to nine fully populated cells to fill your segment of the final design
- Include at least one properly designed popup structure
  - A final report will ask you to predict how you intended it to release and compare it to the end result
- Other designs can be whatever fun images you want
  - Draw -> Layout Generators -> Import Image

Design Guidelines

- Each student can fill up their section of the wafer with their designs
- Any wire you intend to release should be between 10 – 200 microns wide (any more is difficult to undercut enough to release)
  - All areas you intend to release on a single chip should be roughly the same width to ensure simultaneous release (i.e. no 10 micron wide wire connected to a 200 micron wire as the smaller wire will disappear long before the thicker wire releases)
- Ensure some part of your design is anchored
  - Does not have the area underneath etched away
  - May need to include a much thicker area to ensure it doesn't pop off the surface due to stress
- Fill up the die area with your design as many individual instances may fail
  - Possibly include side by side variations with different thicknesses and/or geometry to change rate of curvature and shape

Bubble Trap